Achronix
Data Acceleration

Product Brief

Speedster7t FPGAs

Speedster7t FPGA Highlights

A New Class of FPGA Optimized for High-Bandwidth Workloads

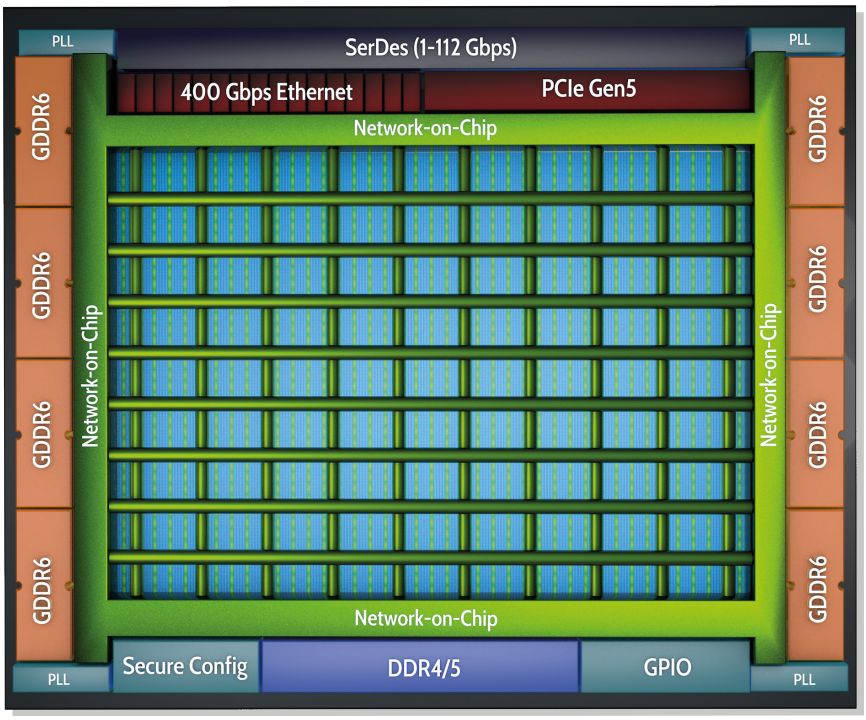
- Built on TSMC 7nm process technology
- 363K to 2.6M 6-input LUTs
- Up to 385 megabits of embedded memory
- Up to 16 GDDR6 channels delivering up to 4 Tbps of memory bandwidth
- Up to 72 SerDes ports supporting data rates of 1 to 112 Gbps
- Up to 4 ports of 400G Ethernet (4× 400G or 16× 100G)
- Up to 4 ports of PCIe Gen5 supporting 16-lane (×16) and 8-lane (×8) configurations
- Revolutionary new 2D network-on-chip (NoC) routing structure that fundamentally changes FPGA design methodologies
- New flexible machine learning processor (MLP) optimized for AI/ML functionality:
  - Delivers up to 41K Int8 MACs and 134 Int8 TOPS
  - Supports multiple floating point and integer numerical formats

An Innovative High-Performance FPGA Family

The Achronix Speedster®7t family is a revolutionary FPGA architecture highly optimized to meet the growing demands of AI/ML and high-bandwidth data acceleration applications. Specifically designed for these high-bandwidth workloads, the Speedster7t FPGA family features a revolutionary new 2D network on chip (NoC) and a high-density array of AI/ML optimized machine learning processors (MLP). Blending FPGA programmability with ASIC routing structures and compute engines, the Speedster7t family creates a new "FPGA+" class of technology.

High-Speed Interfaces Support World-Class Bandwidth

Critical for high-performance compute, machine learning and hardware acceleration is the ability to move data on and off chip, whether it is to support incoming and outgoing data streams, or storing/buffering that data. Speedster7t FPGAs have been architected to support unprecedented bandwidth.



112 Gbps SerDes

Speedster7t devices have up to 72 of the industry's highest performing SerDes interfaces that can operate from 1 to 112 Gbps.

PCI Express Gen5

Speedster7t FPGAs come equipped with multiple PCIe Gen5 interfaces supporting both 16-lane (×16) and 8-lane (×8) configurations. The PCIe controller interfaces support dual operation, as either an endpoint or as a root complex.

Ethernet

Each Speedster7t FPGA includes multiple Ethernet subsystems consisting of 8 SerDes lanes and Ethernet MACs to support a range of applications. Each Ethernet MAC is very flexible and can support multiple ports up to 400G, with

each SerDes lane able to achieve a line rate between 10G and 100G. The high-performance Ethernet interfaces connect to the FPGA fabric through the NoC.

GDDR6

Speedster7t devices are the only FPGAs with embedded support for GDDR6 memories — the highest bandwidth external memory devices available today. Having multiple GDDR6 SDRAM controller ports, Speedster7t FPGAs provide the fastest SDRAM access speeds with the lowest DRAM cost (per stored bit) available.

Each of the GDDR6 memory controllers are capable of supporting 512 Gbps of bandwidth. As a result, the up to 8 GDDR6 controllers in a Speedster7t device can support an aggregate GDDR6 bandwidth of 4 Tbps, delivering the equivalent memory bandwidth of an HBM-based FPGA at a fraction of the cost.

DDR5

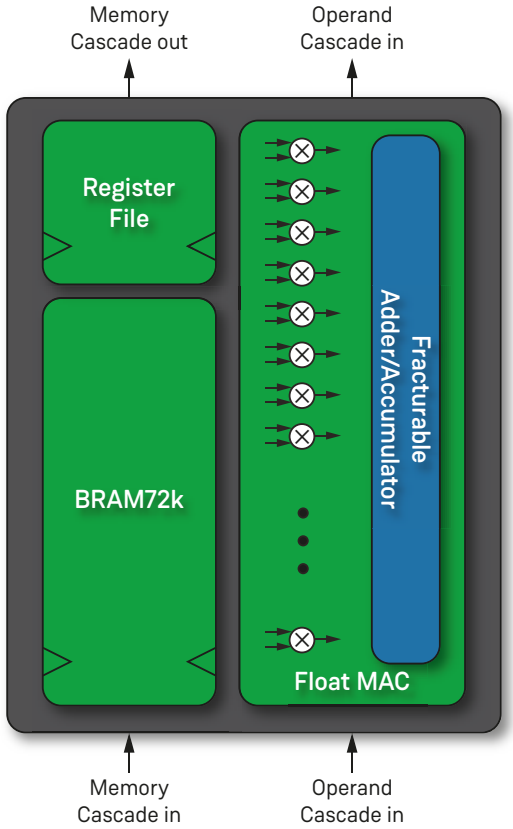
Speedster7t FPGAs include DDR5 memory interface support for deeper buffering requirements. The PHY and controller support multiple configurations such as soldered down components on PCB, UDIMM, SODIMM, RDIMM and LRDIMM modules and bit widths from x4 to x72. The PHY and controller support all standard features defined by the JEDEC specification and are inter-operable with memories from all major vendors. The PHY interface to the hard controller is DFI 4.0 compliant, which allows designers to replace the hard controller with their own soft controller.

New Network On Chip Delivers ASIC-Level Performance

Speedster7t FPGAs feature a revolutionary new 2D network-on-chip (NoC), designed to support the industry's highest performance interface protocols. The NoC also enables direct connections between the various high-speed and memory interfaces. A host processor can transfer data to any of the GDDR6 or DDR5 memory controllers directly from any of the PCIe Gen5 interfaces by simply configuring the NoC for the task. In this use case, none of the FPGA's programmable-logic is consumed because the NoC manages everything — the programmable interconnect within the FPGA array is not required for this data transfer.

The NoC distributes data throughout the FPGA fabric using a series of high-speed row and column network conduits, distributing data traffic horizontally and vertically throughout the FPGA fabric. Each row or column in the NoC has two 256-bit, unidirectional, industry-standard AXI channels operating at a transfer rate of 512 Gbps in each direction.

Speedster7t Machine Learning Processor



Highly Optimized Compute Performance

Each Speedster7t device features a large array of programmable math compute elements, organized into new machine learning processors (MLP) blocks. Each MLP is a highly configurable, compute-intensive block, with up to 32 multiplier/accumulators (MACs), that support integer formats from 4- to 24-bits and various floating-point modes including native support for Tensorflow's Bfloat16 format as well as the highly efficient block floating-point format which dramatically increases performance.

MLP blocks include tightly integrated embedded memory blocks to ensure that machine learning algorithms will run at the maximum performance of 750 MHz. This combination of high-density compute and high-performance data delivery results in a processor fabric that delivers the highest usable FPGA-based tera-operations (TOps) per second.

Security Comes Built In

To confront the threat of third-party attacks, Speedster7t FPGAs come equipped with the most advanced bitstream security features with multiple layers of defense for protecting bitstream secrecy and integrity. Keys are encrypted based on a tamper-resistant physically unclonable function (PUF), and bitstreams are encrypted and authenticated by 256-bit AES-GCM. To defend against side-channel attacks, bitstreams are segmented, with separately derived keys used for each segment, and the decryption hardware employs differential power analysis (DPA) counter measures. Additionally, a 2048-bit RSA public key authentication protocol is used to activate the decryption and authentication hardware. Users can be confident that when they load their secure bitstream, it is the intended configuration because it has been authenticated by RSA public key, AES-GCM private key, and a CRC checksum.

Design Tool Support

Achronix ACE design tools fully support Speedster7t FPGAs today, from design capture to bitstream generation and system debug. Designers can use the powerful floorplanner tool for design optimization and to make regional or site assignments for all design block instances before heading to timing-drive place and route. ACE also includes a critical path analysis tool to analyze timing to ensure a design is meeting its performance specs. Designers also have access to ACE's powerful Snapshot embedded logic analyzer to create complex triggers and show run-time signals within a Speedster7t device.

Proven Conversion Path to Low-Cost ASIC for High-volume Requirements

Achronix is the only company that offers both standalone FPGAs and embedded FPGA IP. Speedcore™ eFPGA IP is the same technology that Achronix uses in its Speedster7t FPGAs, which allows for a seamless conversion from Speedster7t FPGA to ASIC. FPGA applications typically have functions that must remain programmable, while the remainder of the functionality are fixed functions that are dedicated to the specific system application. For ASIC conversions, the fixed functions can be hardened into the ASIC structure, which reduces die size, cost and power. Customers can expect to get up to 50 percent power reduction and 90 percent cost reduction when they use Speedcore eFPGA IP to convert Speedster7t FPGAs to ASIC.

Availability

The Speedster7t FPGA devices range from 363K to 2.6M 6-input LUTs. The ACE design tools that support all of Achronix's products including Speedcore eFPGA and Speedster7t FPGAs are available today.

The first Speedster7t devices and PCIe accelerator boards will be available in Q4 2019.

About Achronix Semiconductor Corporation

Achronix Semiconductor Corporation is a privately held, fabless semiconductor corporation based in Santa Clara, California and offers high-performance FPGA and embedded FPGA (eFPGA) solutions. Achronix's history is one of pushing the boundaries in the high-performance FPGA market. Achronix offerings include programmable FPGA fabrics, discrete high-performance and high-density FPGAs with hardwired system-level blocks, datacenter and HPC hardware accelerator boards, and best-in-class EDA software supporting all Achronix products. The company has sales offices and representatives in the United States, Europe, and China, and has a research and design office in Bangalore, India.

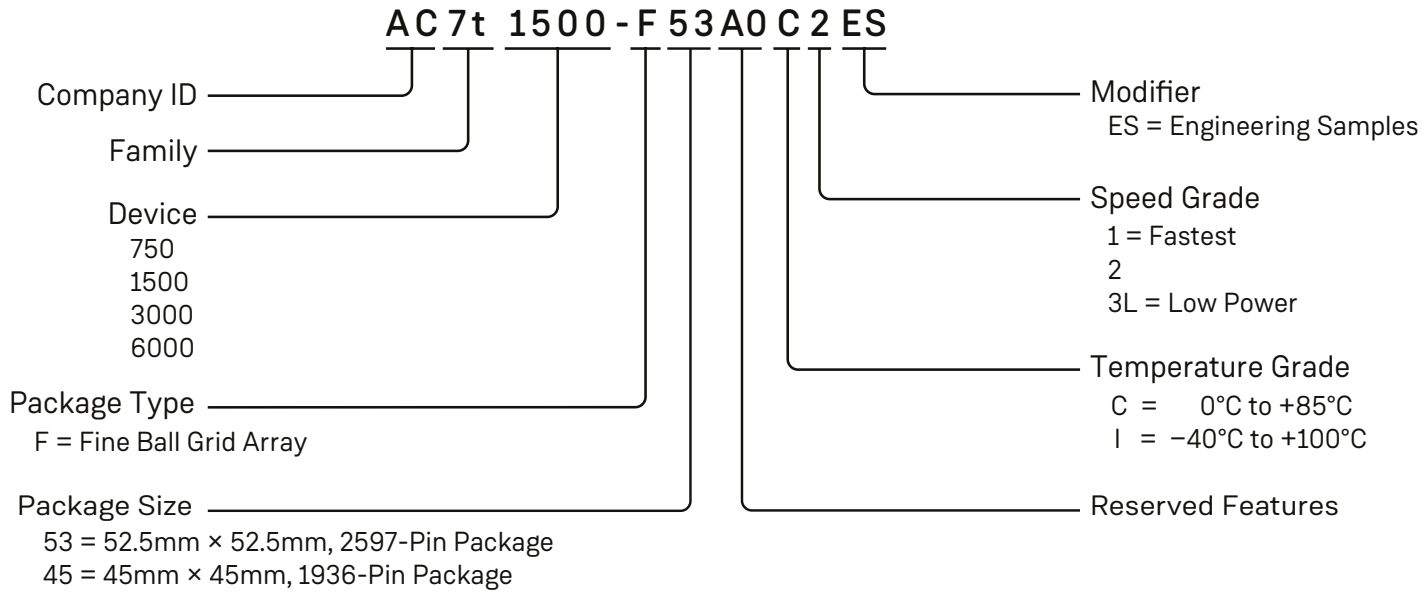
Speedster7t Family Table

Features	AC7t750	AC7t1500	AC7t3000	AC7t6000
6-input LUTs	363K	692K	1.3M	2.6M
Embedded memory	100 Mb	190 Mb	192 Mb	385 Mb
MLP blocks	336	2,560	880	1,760
SerDes 112Gbps (LR + XSR)	24 + 16	32 + 0	40 + 32	72 + 0
Dedicated GPIO	32	64	50	100
Additional GPIO	150	150	300	600
DDR5 channels	1	1†	2	4
GDDR6	8 channels	16 channels‡	16 channels	16 channels
PCIe Gen5	One ×16	One ×16 and one ×8	One ×16 and one ×8	Two ×16
Ethernet	8 lanes, 2×400G or 8×100G	16 lanes, 4×400G or 16×100G	16 lanes, 4×400G or 16×100G	32 lanes, 8×400G or 32×100G

† This device implements DDR4.

‡ This option varies by package size.

Speedster7t Ordering Codes



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