



Stratix 10 Al-optimized FPGA with HBM2

Al-Optimized for High-Bandwidth, Low-Latency Al Acceleration

Designed to tackle the most demanding artificial intelligence workloads, the 520NX is a PCIe card featuring Intel's Stratix 10 NX2100 FPGA. This revolutionary accelerator delivers a unique combination of capabilities needed to implement low latency and larger AI models:

- High-performance Al Tensor Blocks: 143 INT8 TOPS
- Deep Near-Compute Memory: up to 8GB of HBM2
- High-Bandwidth Networking: up to 600Gbps board-to-board bandwidth

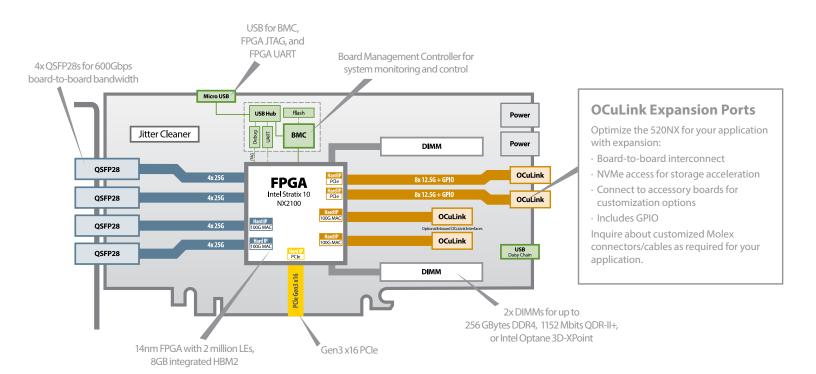
The 520NX features a Board Management Controller (BMC) for advanced system monitoring and control, which greatly simplifies platform integration and management.



key features

Intel Stratix 10 NX2100 8GB of 3D stacked **HBM2**

Al Tensor Blocks



Additional Services

Take advantage of BittWare's range of design, integration, and support options



Customization

Additional specification options or accessory boards to meet your exact needs.



Server Integration

Available pre-integrated in our <u>TeraBox servers</u> in a range of configurations.



Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

FPGA	Intel Stratix 10 NX NX2100 in an F2597 package 8GBytes on-chip High Bandwidth Memory (HBM2) DRAM, 410 GB/s (speed grade 2) Core speed grade -2: I/O speed grade -2 Contact BittWare for other Stratix 10 NX options
On-board Flash	2Gbit Flash memory for booting FPGA
External memory	 2x 288-pin DIMM slots each fitted with 16GB modules by default, i.e., 32GB total on board (options up to 256GB total) Contact BittWare for QDR-II+ & Intel Optane (3D-Xpoint) DIMM options
Host interface	x16 Gen3 interface direct to FPGA, connected to PCIe hard IP
QSFP cages	 4 QSFP28 cages on front panel connected directly to FPGA via 16 transceivers User programmable low jitter clocking supporting 10/25/40/100GbE Each QSFP28 can be independently clocked Jitter cleaner for network recovered clocking 2 QSFP28s have available 100GbE MAC hard IP
OCuLink	 2x edge connectors (A, B) @ 12.5G per lane (default); each supports PCle Gen 3 x8 hard IP, GPIO, and PCle master and optional input clocking 2x inner connectors (C, D) @ 25G per lane (optional); 1x 100GbE MAC hard IP per OCuLink
Board Management Controller	 Voltage, current, temperature monitoring Power sequencing and reset Field upgrades FPGA configuration and control Clock configuration Low bandwidth BMC-FPGA comms with SPI link USB 2.0 PLDM support Voltage overrides

Cooling	 Standard: double-width active heatsink (with fan) Optional: double-width passive heatsink Optional: double-width liquid cooling
Electrical	 On-board power derived from 12V PCle slot & two AUX connectors (one 8-pin, one 6-pin) Power dissipation is application dependent Typical max power consumption 225W
Environmental	Operating temperature: 5°C to 35°C
Quality	 Manufactured to ISO9001:2015 IPC-A-610-Class III RoHS compliant CE, FCC & ICES approvals
Form factor	 Standard-height PCle dual-slot board 4.376 x 10.5 inches (111 x 266.7 mm)

Development Tools

FPGA development	BIST - Built-In Self-Test for CentOS 7 provided with source code (pinout, gateware, PCle driver & host test application)
Application development	Supported design flows - Quartus Prime Pro (HDL, Verilog, VHDL, etc.)

Deliverables

- 520NX FPGA board
- USB cable (front panel access)
- Built-In Self-Test (BIST)
- 1-year access to online Developer Site
- · 1-year hardware warranty





To learn more, visit www.BittWare.com

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