Barcelona Supercomputing Center
Centro Nacional de Supercomputación

EXCELENCIA SEVERO OCHOA

European Commission

EuroHPC Joint Undertaking

# European, extendable, energy-efficient, extreme-scale, extensible, Processor Ecosystem

# (*e*Processor)

***Towards Extreme Scale Technologies and Applications***

***(H2020-JTI-EuroHPC-2019-1 subtopic a)***

11/2020

# Who is involved?

*Starting April 1, 2021, 36 month duration, 8 M€

| | | |
|---|---|---|
| 1 (Coordinator) | Barcelona Supercomputing Center - Centro Nacional de Supercomputación | Spain |
| 2 | Chalmers University of Technology | Sweden |
| 3 | Foundation for Research and Technology Hellas | Greece |
| 4 | Sapienza University of Rome | Italy |
| 5 | **Cortus SAS** | France |
| 6 | **Christmann** | Germany |
| 7 | University of Bielefeld | Germany |
| 8 | **Extoll GmbH** | Germany |
| 9 | **Thales** | France |
| 10 | **EXAscale Performance SYStems p.c.** | Greece |

**Note: Industrial partners in bold.**

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The eProcessor project has received funding from the European High-Performance Computing Joint Undertaking (JU) under grant agreement No. 956702. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Spain, Sweden, Greece, Italy, France, and Germany.

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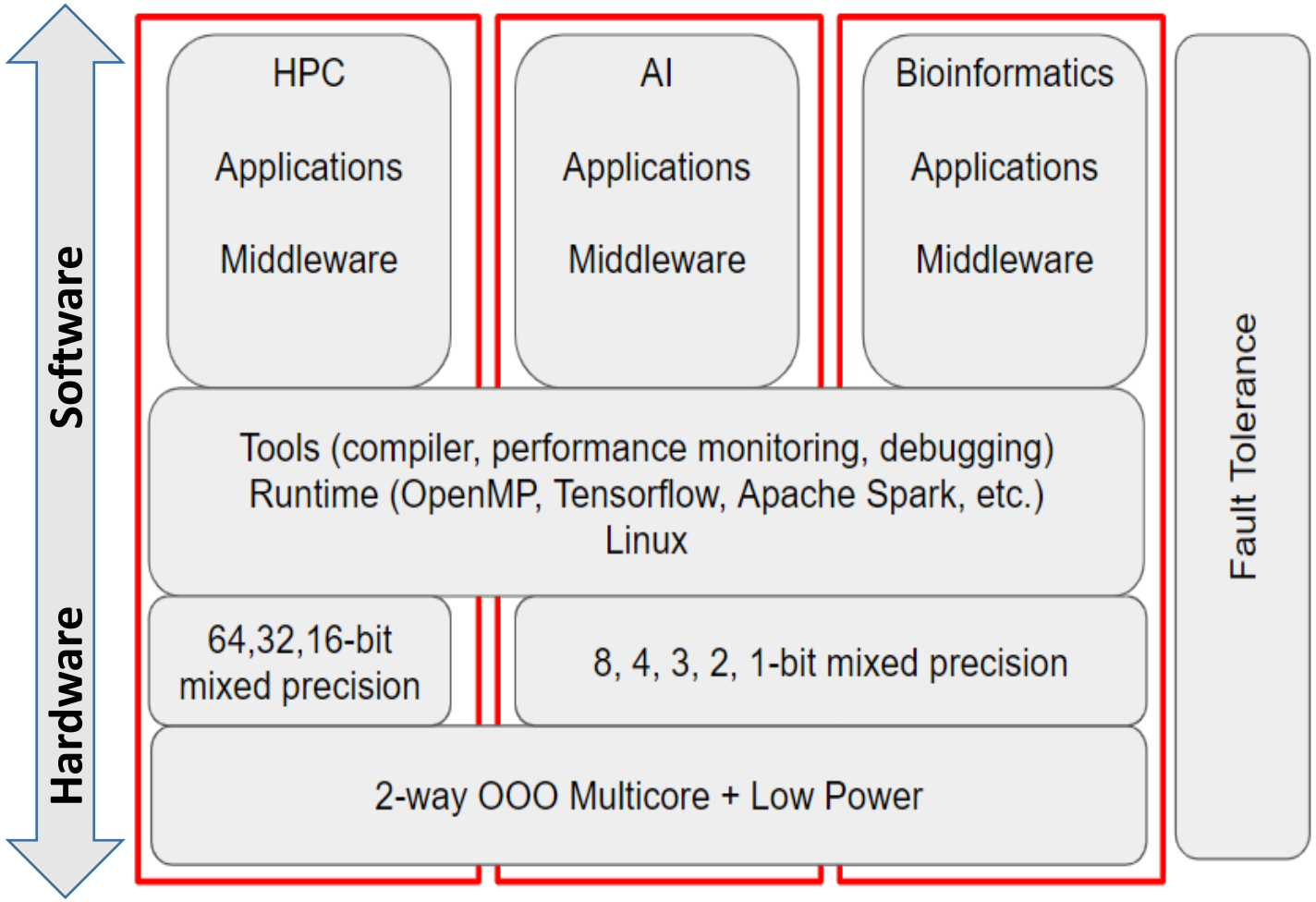
# What is *e*Processor project?

- Software/hardware co-design for improved application performance and system energy efficiency
  - HPC
  - HPDA
  - Bioinformatics
- Europe's first **Open Source** high performance Out-of-Order (OOO) 64-bit RISC-V platform
  - 2-way OOO Core
  - Single core & multi-core tapeouts
  - Multi-socket coherent implementation
  - Adaptive caches
- Vector accelerator
  - New Bioinformatics accelerator co-processor

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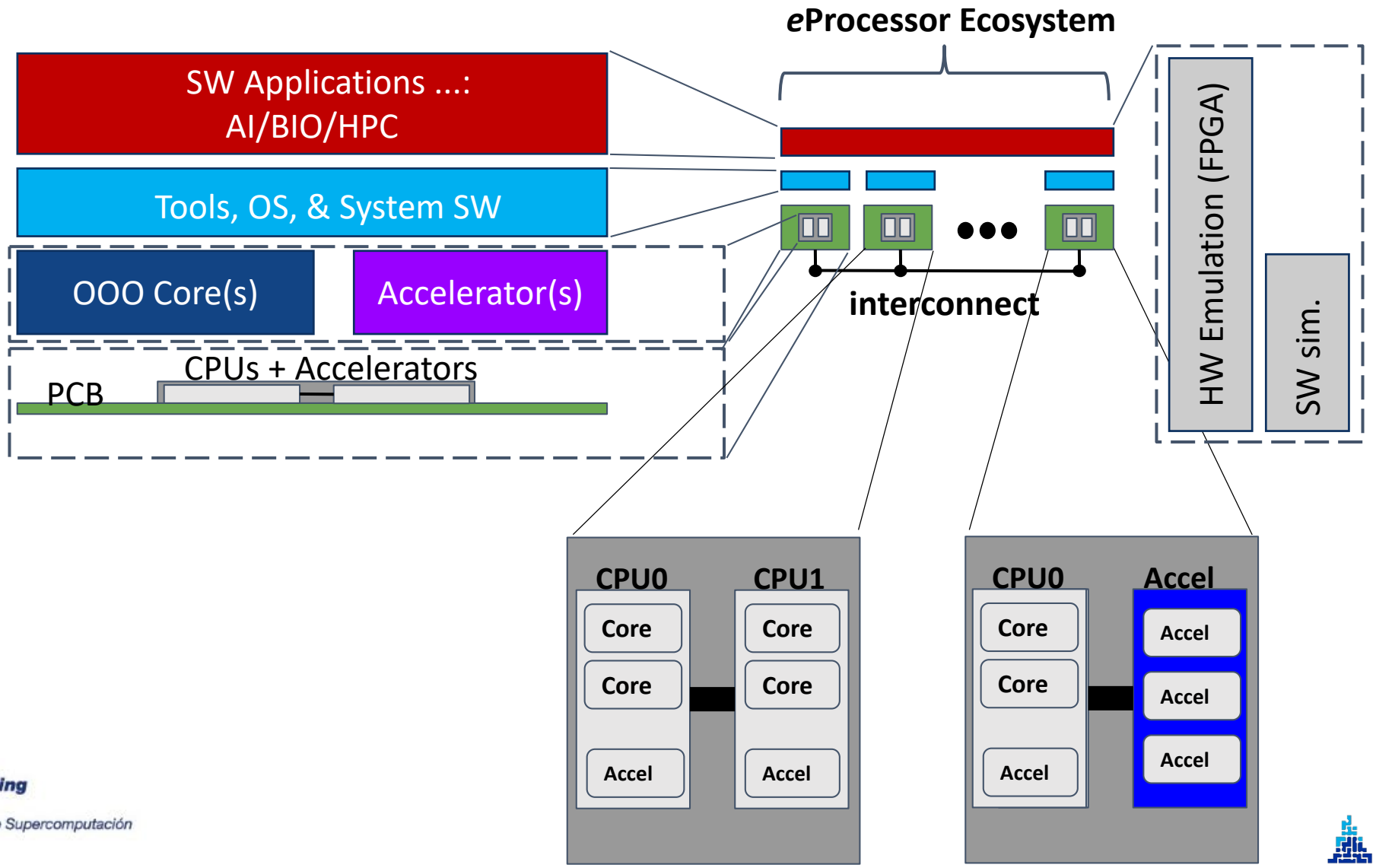
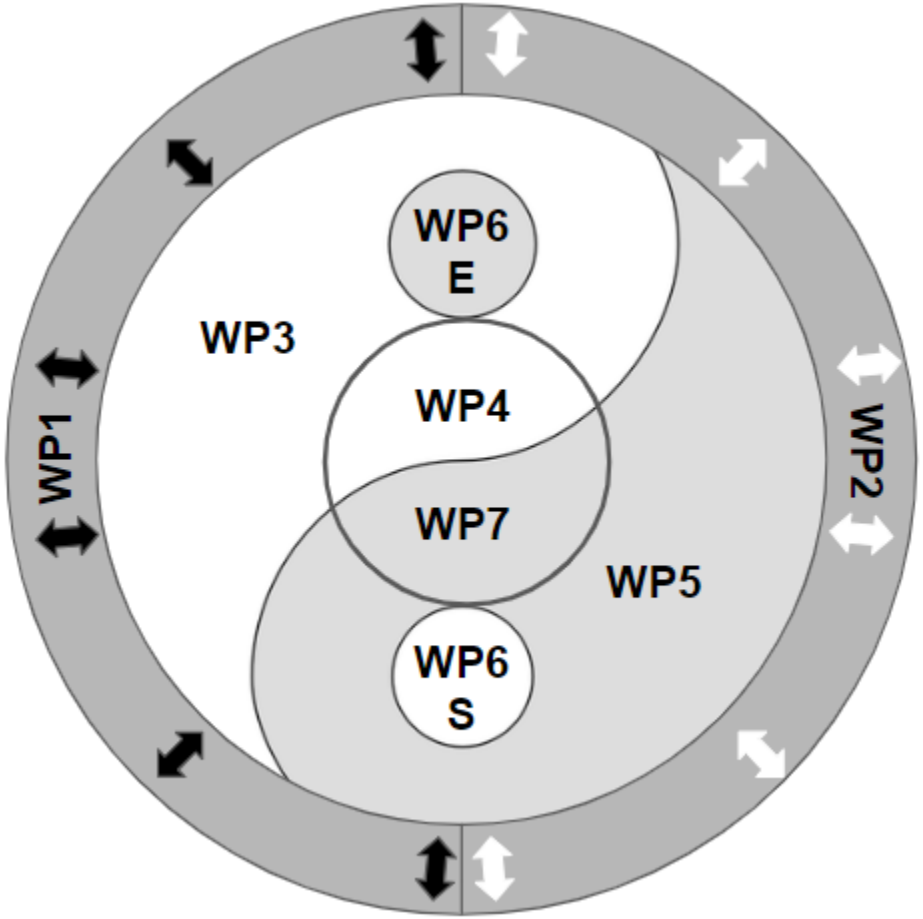
# The *e*Processor Ecosystem



# ePProcessor Work Packages




**WP1**: Coordination & Management
**WP2**: Dissemination & Exploitation
**WP3**: Software Applications Use Cases, Specifications, & Evaluation
**WP4**: Tools, OS, & System Software
**WP5**: Architecture, RTL Design & Verification
**WP6**: (S) System Simulation and (E) FPGA Emulation
**WP7**: Chip Fabrication, PCB development & Validation

SW

HW

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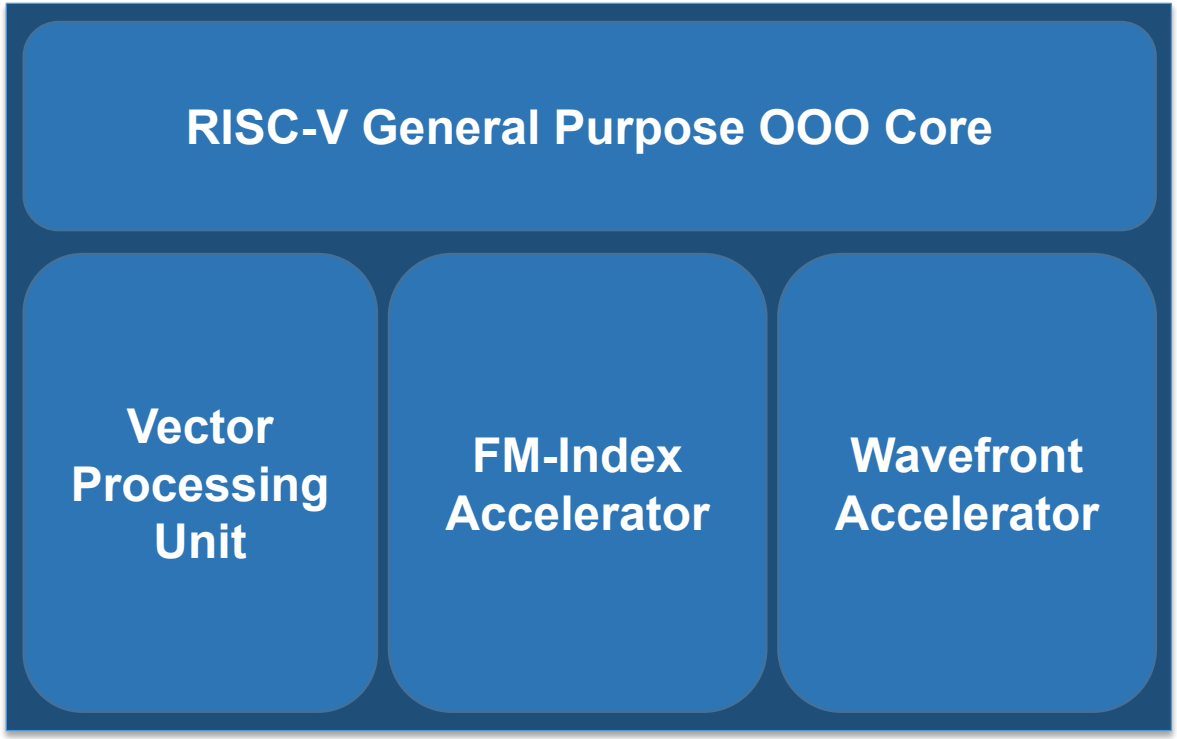
# *e*Processor HW accelerator for genome mapping

**Main goal: design a general purpose RISC-V OOO processor and a tightly-coupled accelerator for genome mapping**



# *e*Processor Acceleration Techniques

- Vector extensions following RISC-V Vector Working Group
  - Baseline implementation following EPI Vector Processing Unit (VPU) design
  - Develop 2, 4, 8-bit artihmetic instructions for genomics
  - Memory operations  to pack/unpack 32/64-bit to 2/4/8-bit elements
- Bit manipulation extensions following RISC-V Bitmanip Working Group
  - Bit manipulation, compute parity of a word (popcount, dot product)
- Specialized instructions
  - shrd: Shifts MSB of one register to LSB of another, used to combine two multiplications
  - PCLMULQDQ, VMULLp64: Carry-less multiplication of 64-bit operands
  - UMULL: Multiplication of 32-bit unsigned integer operands
- Hardware modules, hardware/software co-design
- Main objective: develop custom accelerator for genome mapping and demonstrate their performance benefits.

# MareNostrum5 R&D → MEEP:HW Emulator → eProcessor

(MareNostrum Experimental Exascale Platform)

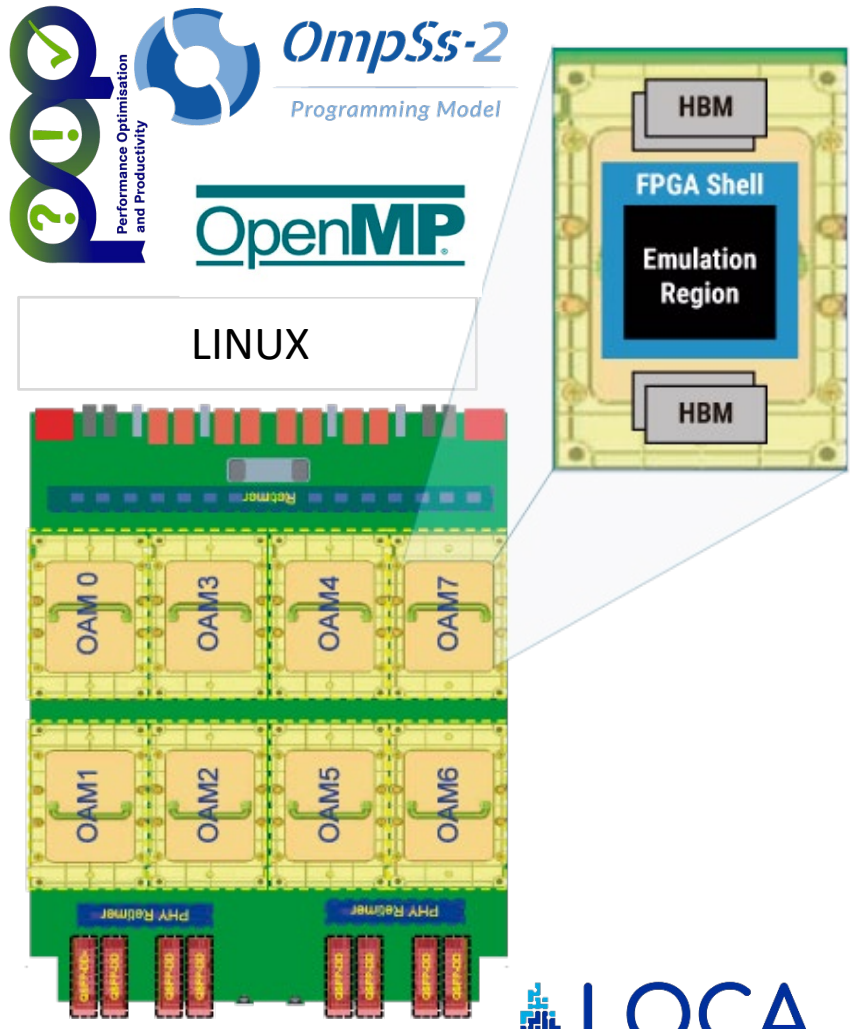
**Large-scale Emulations for Exascale Systems**

Software stack development vehicle
- Apps down to OS and tools

FPGA Emulation Platform
- Open Compute Accelerator Module (OAM) FPGA + HBM
  - RISC-V: Scalar+DLP accelerators+Memory

Develop & Improve Technology Readiness Level (TRL):
- RISC-V: Scalar + Vector (and other DLP accelerator) cores
- Memory hierarchy
- Software stack

IoT to HPC, AI/ML/DL

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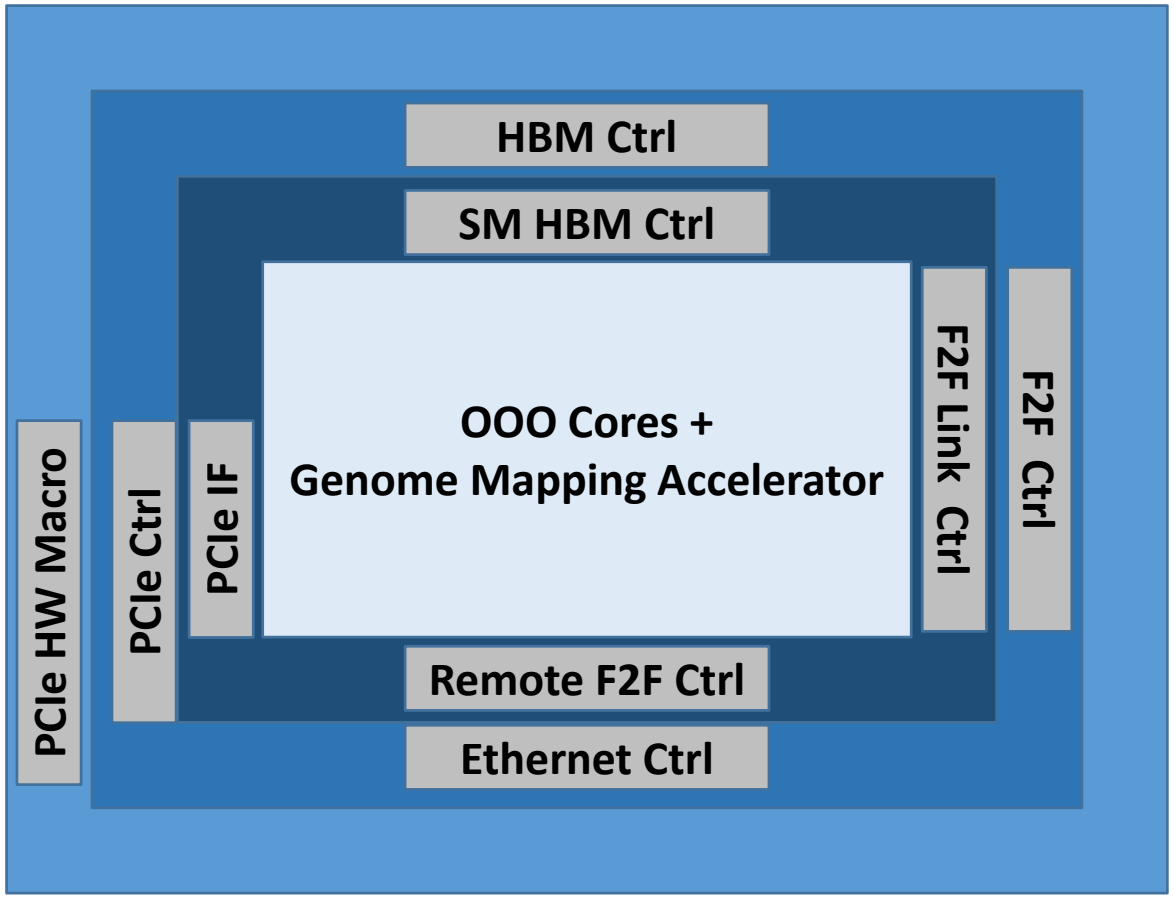
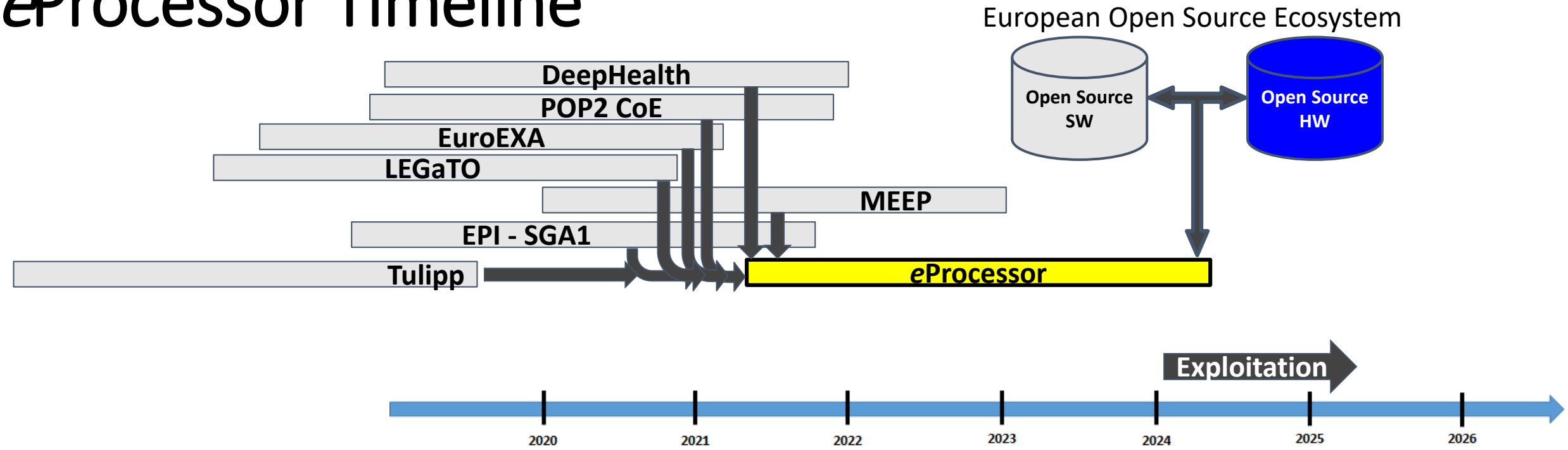
# *e*Processor Emulator Target: OOO Cores + Genome Mapping Accelerator

- FPGA target: Xilinx Alveo U280
  - Match Phase 1 of MEEP
- Xilinx FPGA Shell
  - PCIe interface to the Host machine
  - HBM memory
  - FPGA-2-FPGA Links
  - 100 Gb Ethernet
- OOO Cores
- Genome Mapping Accelerator



# *e*Processor Timeline




- LEGaTO: COM Express PCB for LEGaTO HPC System
- MEEP: FPGA Emulator
- EPI: IP for the Vector Accelerator, L2 Cache, etc.
- Tulipp: Optimizations for performance/watt

- DeepHealth: DL and CV libraries
- POP: SW Profiling and tools
- EuroEXA & Exa*: Extend previous work for IO-coherence and IOMMU

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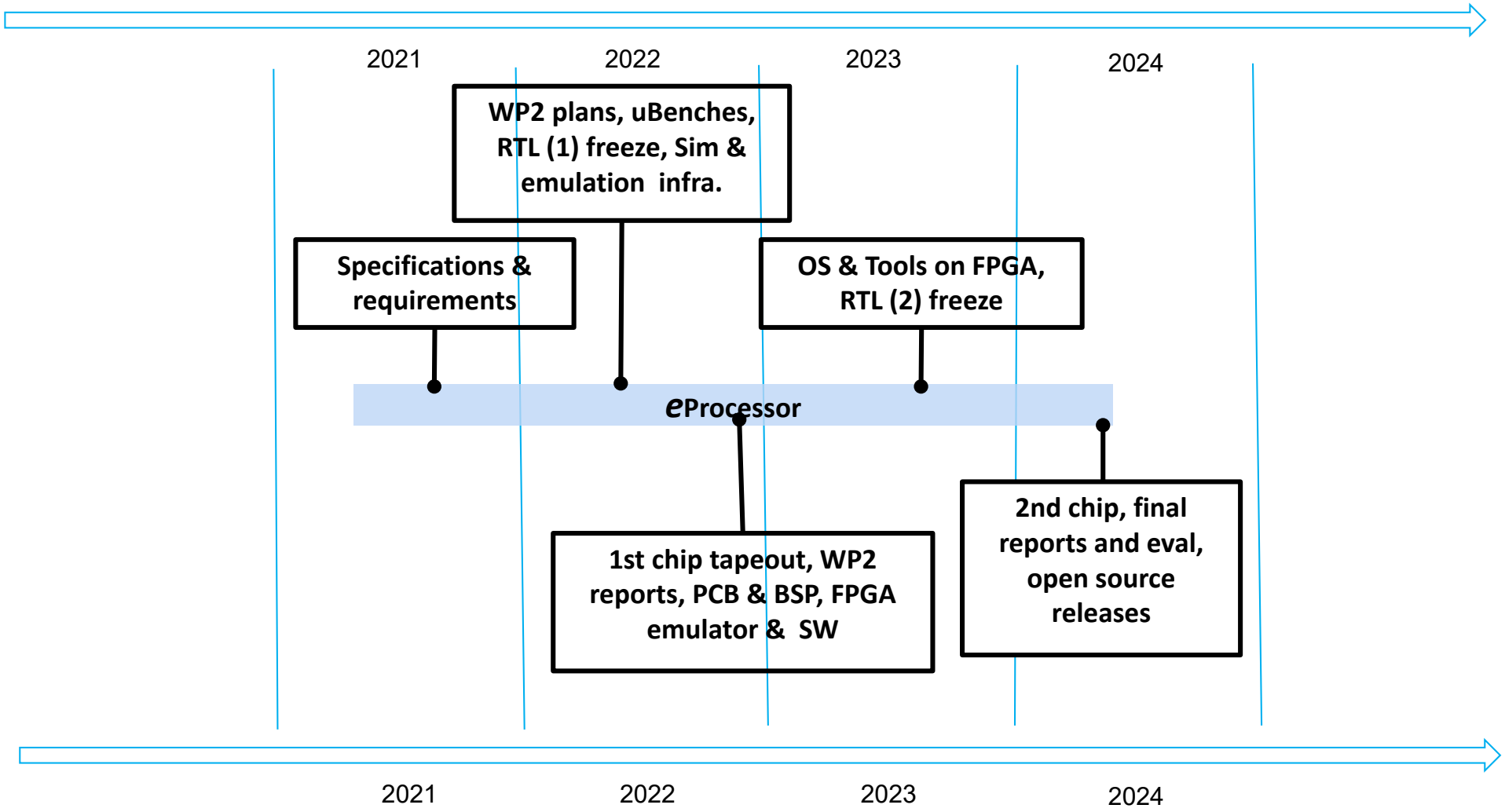
# ePProcessor Milestones




*Starting April 2021

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# *e*Processor Impact

- Europe's First Open Source Out of Order RISC-V Processor
  - Single core implementation
  - Dual core implementation
- Internal coprocessor accelerator
  - Vector coprocessor (Extending EPI)
  - Bioinformatics/HPC/AI coprocessor
- External Coherent Link
  - Dual socket CPUs
  - Coherent external accelerator link
- LEGaTO Platform
  - Leverage the COM Express and LEGaTO HPC system

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# Thank you

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