MONT-BLANC 2020

Our mission:

Pave the way to a power-efficient European processor for HPC and beyond

The Mont-Blanc DNA

Inherited from the three previous Mont-Blanc projects:

- Economic sustainability
- Power efficiency
- Heterogeneity
- Strong codesign approach for real applications
- Building a prototype

Mont-Blanc 2020 main choices

- Use the **Arm ISA**
- Design, implement and leverage new technologies to improve the performance, power efficiency, reliability and security of the processor:
  - large SVE compute units
  - specific NoC
  - specific High Bandwidth Memory controller
  - specific SoC Power Management controller
  - innovative packaging technologies (Interposer)
  - state of the art silicon process 7nm FF
- Improve the economic sustainability of processor development through a **modular design** that allows to retarget our SoC for **different markets** adding specific accelerators

Project Objectives

Mont-Blanc 2020 will provide **new IPs**, such as **a new low-power mesh interconnect** based on the Coherent Hub Interface (CHI) architecture:

- supporting **up to 128 low power HPC cores;**
- each core embedding **2 vector units from 128 to 1024 bits wide;**
- interfacing HBM3 memory controllers to sustain **up to 2TB/s** of memory bandwidth.

Mont-Blanc 2020 will **demonstrate the performance:**

- Power, Performance and Area (PPA) **metrics in 7nm,**
- **prototype implementation in RTL** for some of its keycomponents and demonstration on an emulation platform,
- 'embedded processing' **POC on FPGA**.

3 Key Challenges

To achieve the **desired performance** with the **targeted power consumption,** the project will need to tackle these challenges:

1. understand the **trade-offs between vector length, NoC bandwidth and memory bandwidth** to maximize processing unit efficiency;
2. an **innovative on-die interconnect** that can deliver enough bandwidth with minimum energy consumption;
3. a **high-bandwidth / low power memory solution** with enough capacity and bandwidth for Exascale applications.

What's next?

Mont-Blanc 2020 is **at the heart of the European exascale supercomputer effort,** since most of the IP developed within Mont-Blanc 2020 will be reused and productized in the **European Processor Initiative (EPI).**

European Processor Initiative

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