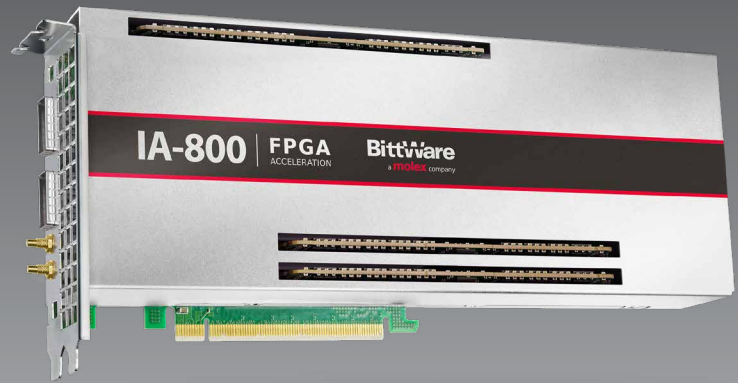


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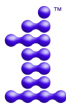
IA-840F
PCIe FPGA Board



Agilex™ FPGA card with QSFP-DD and MCIO

4x 100GbE with up to 384GB of DDR4 SDRAM

BittWare's IA-840F is an Intel® Agilex™-based FPGA card designed to deliver up to 40% higher performance for data center, networking and edge compute workloads. BittWare maximized I/O features on the card using the Agilex chip's unique tiling architecture with dual QSFP-DDs (4x 100G), PCIe Gen4 x16, and three MCIO expansion ports for diverse applications. The card also supports Intel oneAPI™, which enables an abstracted development flow for dramatically simplified code re-use across multiple architectures.


oneAPI



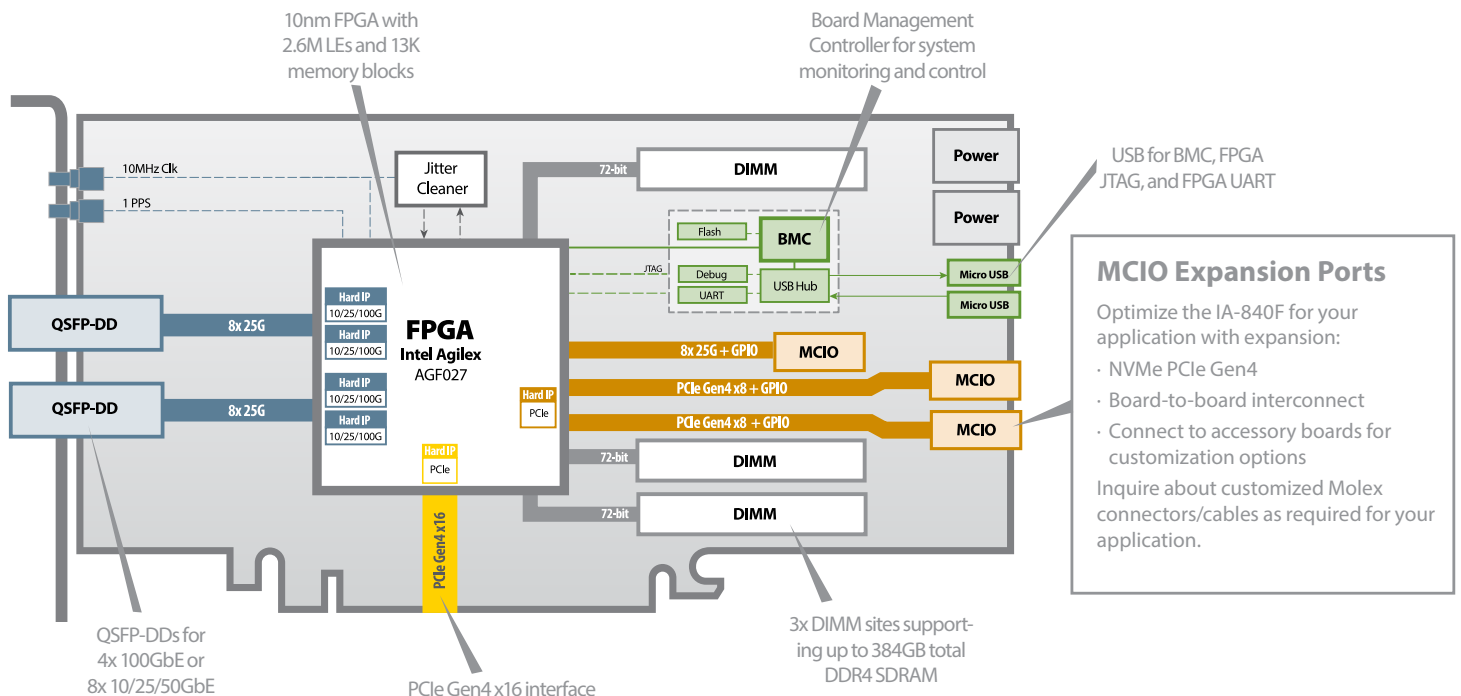
The IA-840F supports Intel's OneAPI open standards-based unified programming model

key features

QSFP-DDs
for 4x 100G or
16x 10/25G

**Intel
OneAPI**
support

Intel Agilex™ FPGA
with up to **2.6M**
Logic Elements



Additional Services

Take advantage of BittWare's range of design, integration, and support options



Customization

Additional specification options or accessory boards to meet your exact needs.



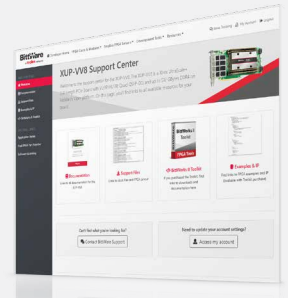
Server Integration

Available pre-integrated in our [TeraBox servers](#) in a range of configurations.



Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

FPGA	- Intel Agilex - AGF027 in an R2581A package - Core speed grade -2: I/O speed grade -2 - Contact BittWare for other Agilex FPGA options
On-board Flash	2Gbit Flash memory for booting FPGA
External memory	3x 288-pin DIMM slots, each supporting up to 128GB DDR4 SDRAM modules (up to 384GB total) - Designed-in support for other DIMM modules such as QDR SRAM and Optane. Contact BittWare for details.
Host interface	x16 Gen4 interface direct to FPGA, connected to PCIe hard IP
QSFP-DD cages	2 QSFP-DD cages on front panel connected directly to FPGA via 16 transceivers - User programmable low jitter clocking supporting 10/25/40/100GbE - Each QSFP-DD can be independently clocked - Jitter cleaner for network recovered clocking - Multi-rate hard MAC+FEC for 10/25/100GbE
MCIO	2x edge connectors supporting 8x 16G plus GPIO sidebands; supports 4x Gen4 x4 PCIe root complexes, 2x Gen4 x8 endpoints, or 1x Gen4 x16 root complex or endpoint 1x inner connector supporting 8x 25G plus GPIO sidebands
External clocking	1 PPS and 10MHz ref clk front panel inputs
USB Micro	USB access to BMC, USB-JTAG, USB-UART

Board Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- Low bandwidth BMC-FPGA comms with SPI link
- USB 2.0
- PLDM support
- Voltage overrides

Cooling

- Standard: double-width passive heatsink
- Optional: double-width active heatsink (with fan)
- Optional: double-width liquid cooling

Electrical

- On-board power derived from 12V PCIe slot & two AUX connectors
- Power dissipation is application dependent
- Typical max power consumption TBD

Environmental

- Operating temperature: 5°C to 35°C

Quality

- Manufactured to ISO9001:2015 IPC-A-610-Class III
- RoHS compliant
- CE, FCC & ICES approvals

Form factor

- Standard-height PCIe dual-slot board
- 4.376 x 10.5 inches (111 x 266.7 mm)

Development Tools

System development	BittWare SDK including PCIe driver, libraries, and board monitoring utilities
Application development	Supported design flows - Intel FPGA oneAPI Base Toolkit, Intel High-Level Synthesis (C/C++) & Quartus Prime Pro (HDL, Verilog, VHDL, etc.)



FPGA Design
Solutions Network
Platinum

To learn more, visit www.BittWare.com

Rev 2020.11.16 | November 2020

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Designed to tackle the most demanding artificial intelligence workloads, the 520NX is a PCIe card featuring Intel's Stratix 10 NX2100 FPGA. This revolutionary accelerator delivers a unique combination of capabilities needed to implement low latency and larger AI models:

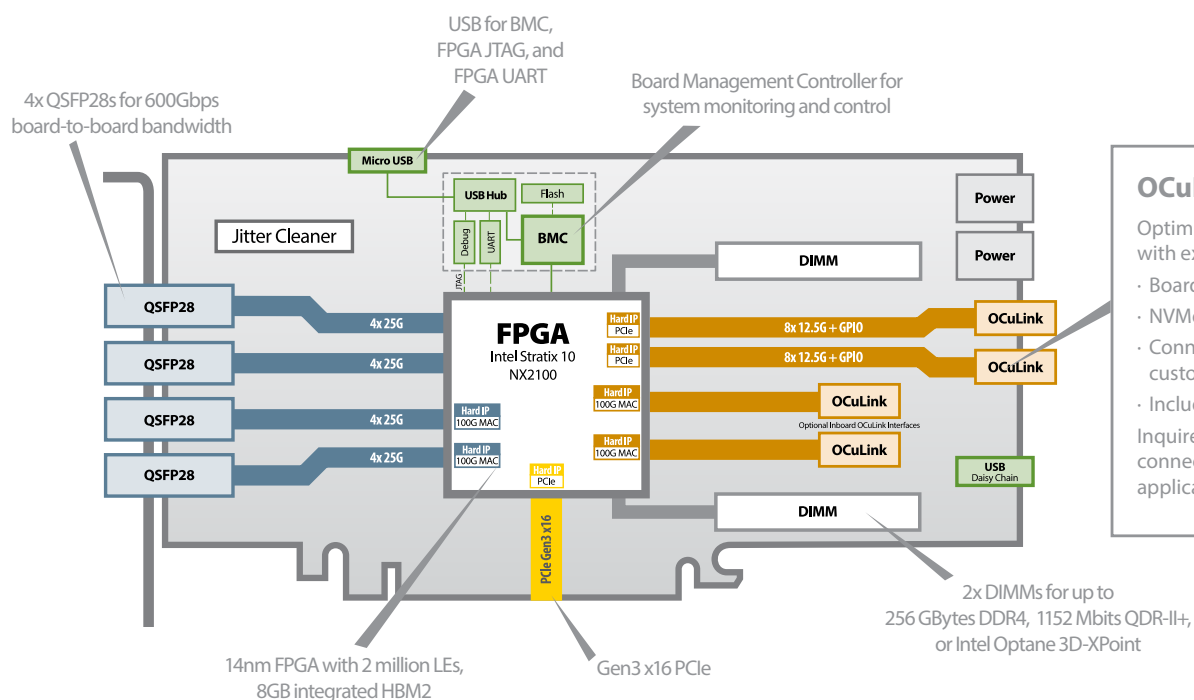
- The 520NX features a Board Management Controller (BMC) for advanced system monitoring and control, which greatly simplifies platform integration and management.



Intel Stratix 10 NX2100

8GB of 3D
stacked **HBM2**

AI Tensor Blocks



OCuLink Expansion Ports

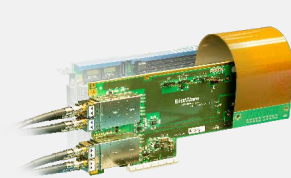
Optimize the 520NX for your application with expansion:

- Board-to-board interconnect
- NVMe access for storage acceleration
- Connect to accessory boards for customization options
- Includes GPIO

Inquire about customized Molex connectors/cables as required for your application.

Additional Services

Take advantage of BittWare's range of design, integration, and support options



Customization

Additional specification options or accessory boards to meet your exact needs.



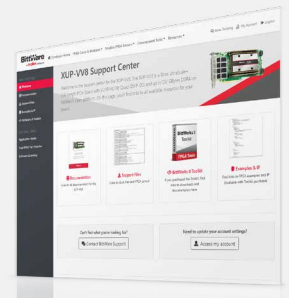
Server Integration

Available pre-integrated in our [TeraBox servers](#) in a range of configurations.



Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

FPGA	- Intel Stratix 10 NX - NX2100 in an F2597 package 8GBytes on-chip High Bandwidth Memory (HBM2) DRAM, 410 GB/s (speed grade 2) - Core speed grade -2: I/O speed grade -2 - Contact BittWare for other Stratix 10 NX options
On-board Flash	2Gbit Flash memory for booting FPGA
External memory	2x 288-pin DIMM slots each fitted with 16GB modules by default, i.e., 32GB total on board (options up to 256GB total) - Contact BittWare for QDR-II+ & Intel Optane (3D-Xpoint) DIMM options
Host interface	x16 Gen3 interface direct to FPGA, connected to PCIe hard IP
QSFP cages	4 QSFP28 cages on front panel connected directly to FPGA via 16 transceivers - User programmable low jitter clocking supporting 10/25/40/100GbE - Each QSFP28 can be independently clocked - Jitter cleaner for network recovered clocking 2 QSFP28s have available 100GbE MAC hard IP
OCuLink	2x edge connectors (A, B) @ 12.5G per lane (default); each supports PCIe Gen 3 x8 hard IP, GPIO, and PCIe master and optional input clocking 2x inner connectors (C, D) @ 25G per lane (optional); 1x 100GbE MAC hard IP per OcuLink
Board Management Controller	- Voltage, current, temperature monitoring - Power sequencing and reset - Field upgrades - FPGA configuration and control - Clock configuration - Low bandwidth BMC-FPGA comms with SPI link - USB 2.0 - PLDM support - Voltage overrides

Cooling	- Standard: double-width active heatsink (with fan) - Optional: double-width passive heatsink - Optional: double-width liquid cooling
Electrical	- On-board power derived from 12V PCIe slot & two AUX connectors (one 8-pin, one 6-pin) - Power dissipation is application dependent - Typical max power consumption 225W
Environmental	Operating temperature: 5°C to 35°C
Quality	- Manufactured to ISO9001:2015 IPC-A-610-Class III - RoHS compliant - CE, FCC & ICES approvals
Form factor	- Standard-height PCIe dual-slot board 4.376 x 10.5 inches (111 x 266.7 mm)

Development Tools

FPGA development	BIST - Built-In Self-Test for CentOS 7 provided with source code (pinout, gateway, PCIe driver & host test application)
Application development	Supported design flows - Quartus Prime Pro (HDL, Verilog, VHDL, etc.)

Deliverables

- 520NX FPGA board
- USB cable (front panel access)
- Built-In Self-Test (BIST)
- 1-year access to online Developer Site
- 1-year hardware warranty



FPGA Design
Solutions Network
Platinum

To learn more, visit www.BittWare.com

Rev 2020.11.16 | November 2020

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254-U2
U.2 FPGA Accelerator

UltraScale+ on U.2 Form Factor with PCIe Gen4

FPGA-Based Computational Storage Processor for NVMe Acceleration

BittWare's 254-U2 is a Computational Storage Processor conforming to the U.2 form factor. Ideal for NVMe acceleration, it features a Xilinx Kintex UltraScale+ FPGA supporting PCIe Gen4 directly coupled to local DDR4 memory. This energy-efficient, flexible compute node is intended to be deployed within conventional U.2 NVMe storage arrays (approximately 1:8 ratio) allowing FPGA-accelerated instances of:

- Erasure Coding and Deduplication
- Compression, Encryption & Hashing
- String/Image Search and Database Sort/ Join/Filter
- Machine Learning Inference

The 254-U2 can be wholly programmed by customers developing in-house capabilities or delivered as a ready-to-run pre-configured solution featuring Eideticom's NoLoad® IP. The 254-U2 is front-serviceable in a 1U chassis and can be mixed in with storage units in the same server, allowing users to mix-and-match storage and acceleration.

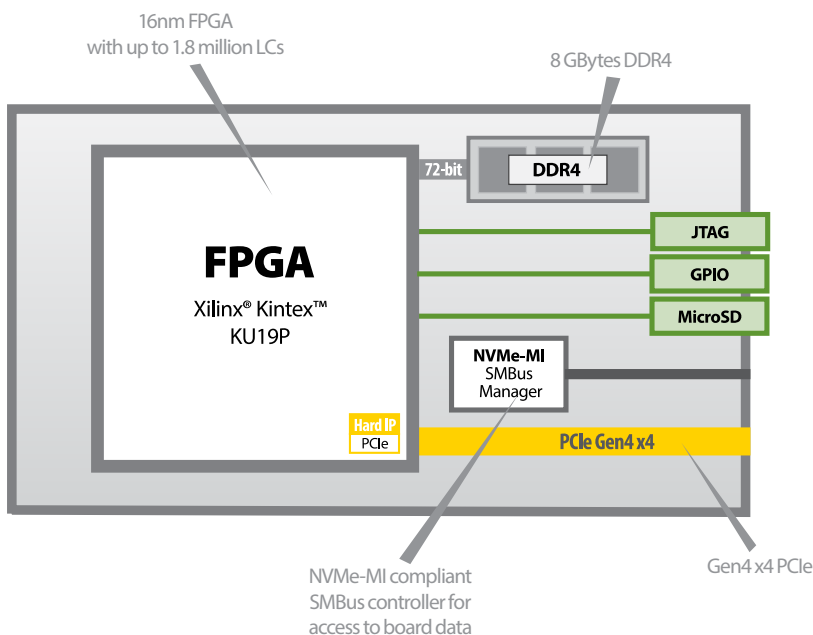


key features

KU19P FPGA:
1.8 million LCs
Kintex UltraScale+

PCIe Gen4
Support

Up to
16 GBytes
DDR4



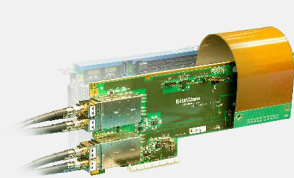
Order your 254-U2 pre-configured with Eideticom's NoLoad:

- Plug-and-play solution
- NVMe compatible and standards-based with no OS changes
- Reduced TCO/TCA - lower power and reduced IO
- CPU offload improves QoS up to 40x
- Disaggregates compute and storage into independently scalable resources
- CPU agnostic
- Reconfigurable accelerators, enabling scalable compute architectures

Learn more at www.eideticom.com

Additional Services

Take advantage of BittWare's range of design, integration, and support options



Customization

Additional specification options or accessory boards to meet your exact needs.



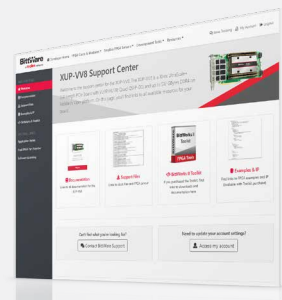
Server Integration

Available pre-integrated in our [TeraBox servers](#) in a range of configurations.



Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Specifications

FPGA	- Xilinx Kintex UltraScale+ - KU19P in an FFVB2104 package - Core speed grade -2 - Contact BittWare for other FPGA options
On-board DDR4 SDRAM	- One bank of DDR4 SDRAM x 72 bits 8GB bank (16GB version also available) - Transfer Rate: 2400 MT/s
Host interface	- PCIe Gen4 x4 - U.2 Connector - Compliant to SFF-8639
Datacenter deployment	- On-board NVMe-MI compliant SMBus controller (Spec. 1.0a) - Field flash update via software or SMBus - SMBus FPGA flash control: anti-bricking, fallback and multiboot - SMBus access to unique board data and temperature sensor
Back panel features	- User LEDs accessible - Reset switch to restore factory settings
Development features	- JTAG connector for access to the FPGA, flash and debug tools - GPIO connector - MicroSD connector
Power supply monitoring & reporting	- Voltage monitoring - Temperature monitoring - Fault condition reporting to FPGA

Cooling	U.2 drive case optimized for cooling with passive heatsink
Electrical	- Hot swapping tolerant - On-card power derived from U.2 supplies - Power dissipation is application dependent - Typical FPGA power consumption ~20W - Card designed to deliver up to 25W power consumption
Environmental	- Operating temperature: 5°C to 35°C - Cooling: air convection
Quality	- Manufactured to ISO9001:2008 IPC JSTD-001 -Class III - RoHS compliant
Form factor	- U.2 compliant 2.5" Drive Form Factor - Height: 15mm

Development Tools

FPGA development	BIST - Built-In Self-Test for CentOS 7 provided with source code (pinout, gateware, PCIe driver and host test application)
Application development	Xilinx Tools - Vivado Design Suite HLx Editions: HDL and C/C++ with HLS

Deliverables

- 254-U2 FPGA board
- Built-In Self-Test (BIST)
- Eideticom NoLoad pre-installed (optional)
- 1-year access to online Developer Site
- 1-year hardware warranty
- Contact BittWare for extended warranty and support options

To learn more, visit www.BittWare.com

Rev 2020.10.26 | October 2020

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250-M2D M.2 Accelerator Module



M.2 Accelerator Module with Xilinx® UltraScale+™ FPGA

The BittWare 250-M2D is an FPGA-based Computational Storage Processor (CSP) designed to meet the draft M.2 Accelerator Module Hardware Specification standard*. It is intended to operate in Glacier Point carrier cards for Yosemite servers. These feature-rich, dense servers are favored by hyperscale and cloud companies striving to improve the performance density and energy-efficiency of machine learning platforms.

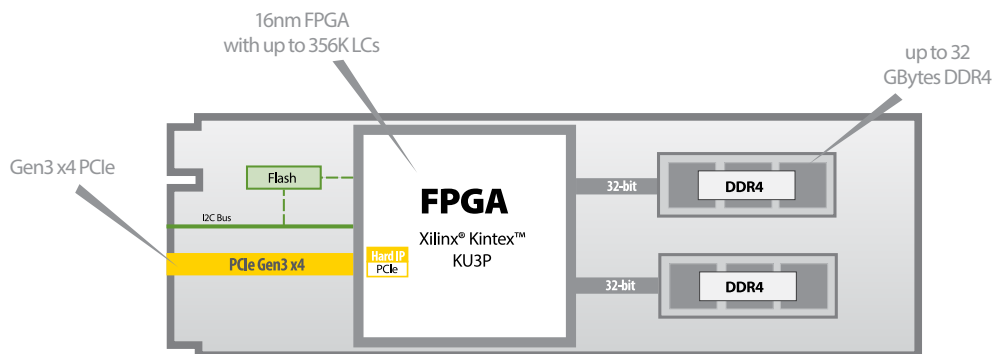
The 250-M2D product features a Xilinx Kintex® UltraScale+ FPGA directly coupled to two banks of local DDR4 memory. Customers can either develop their own acceleration applications in HDL, or take advantage of pre-programmed accelerator solutions featuring IP from BittWare partner companies.

key features

Ideal for
**Computational
Storage**

KU3P FPGA:
356K LCs
Kintex UltraScale+

Up to
32 GBytes
DDR4



Myrtle.ai

Order your 250-M2D pre-configured with the Myrtle.ai SEAL accelerator for recommender systems:

- Rapid 8x scaling in processing capacity with the same server infrastructure
- 50% less CapEx required to build new processing capacity
- More content ranking within tight latency constraints means better recommendations and hence increased revenue
- Up to 80% reduction in energy consumption
- Easy to install
- Complementary to other accelerators
- Scalable

Learn more at www.myrtle.ai/SEAL



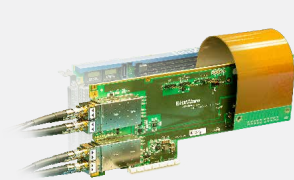
Order your 250-M2D pre-configured with Eideticom's NoLoad:

- Plug-and-play solution
- NVMe compatible and standards-based with no OS changes
- Reduced TCO/TCA - lower power and reduced IO
- CPU offload improves QoS up to 40x
- Disaggregates compute and storage into independently scalable resources
- CPU agnostic
- Reconfigurable accelerators, enabling scalable compute architectures

Learn more at www.eideticom.com

Additional Services

Take advantage of BittWare's range of design, integration, and support options



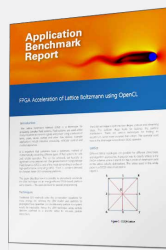
Customization

Additional specification options or accessory boards to meet your exact needs.



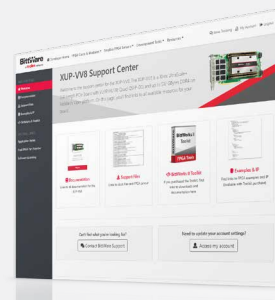
Server Integration

Available pre-integrated in our [TeraBox servers](#) in a range of configurations.



Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Specifications

FPGA	- Xilinx Kintex UltraScale+ - KU3P in an B784 package - Core speed grade -2 - Contact BittWare for additional FPGA options
On-board DDR4 SDRAM	- Two banks of DDR4 SDRAM x 32 bits 8GB bank (16GB version also available) - Transfer Rate: up to 2400 MT/s
Host interface	M.2 interface supporting Gen3 x4 PCIe
Cooling	Open Compute M.2 accelerator case optimized for cooling with passive heatsink
Electrical	- Hot swapping tolerant - Power dissipation is application dependent - TDP: 14.85W max - Module Absolute Peak Power (20us): 24W

Environmental	- Operating temperature: 5°C to 50°C at module inlet - Cooling: air convection
Quality	- Manufactured to ISO9001:2008 IPC JSTD-001 -Class III - RoHS compliant
Form factor	- M.2 Accelerator Module Hardware Specification* (not designed for standard M.2) * Opencompute.org/wiki/Server/Working

Development Tools

FPGA development	BIST - Built-In Self-Test for CentOS 7 provided with source code (pinout, gateway, PCIe driver and host test application)
Application development	Xilinx Tools - Vivado Design Suite HLx Editions: HDL and C/C++ with HLS
PCIe carrier card	PCIe carrier card allowing 250-M2D to be populated in a standard PCIe slot for lab development

Deliverables

- 250-M2D FPGA board
- Built-In Self-Test (BIST)
- Eideticom NoLoad pre-installed (optional)
- Myrtle.ai SEAL pre-installed (optional)
- 1-year access to online Developer Site
- 1-year hardware warranty
- Contact BittWare for extended warranty and support options

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RFX-8440 PCIe RFSoc Board



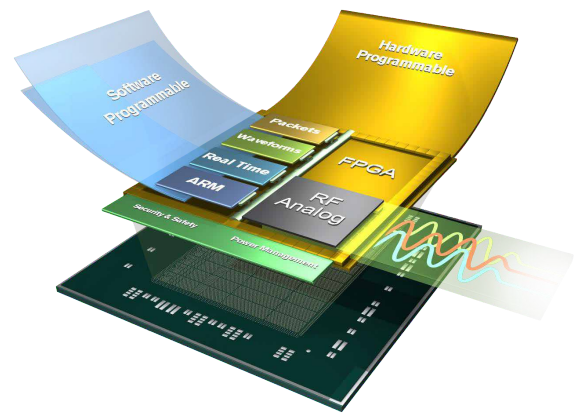
Zynq RFSoc PCIe & Standalone Platform

Seamlessly cross between analog and digital at up to gigahertz rates

The BittWare RFX-8440 data acquisition card features the third generation Xilinx Zynq® UltraScale+™ RFSoc. This innovative PCIe data acquisition card is capable of addressing the entire sub-6 gigahertz (GHz) spectrum – a critical need for applications such as 5G, LTE wireless, phased array RADAR and satellite communications.

The Xilinx Zynq® UltraScale+™ RFSoc integrates RF-class A/D and D/A converters into the Zynq® FPGA fabric and multi-core ARM processor subsystem, creating a multi-channel data conversion and processing solution on a single chip.

With the product development, manufacturing, quality and lifecycle management capabilities of the Molex group behind it, the RFX-8440 is an Enterprise-class product ideal for rapid prototyping as well as volume deployment in end user systems.

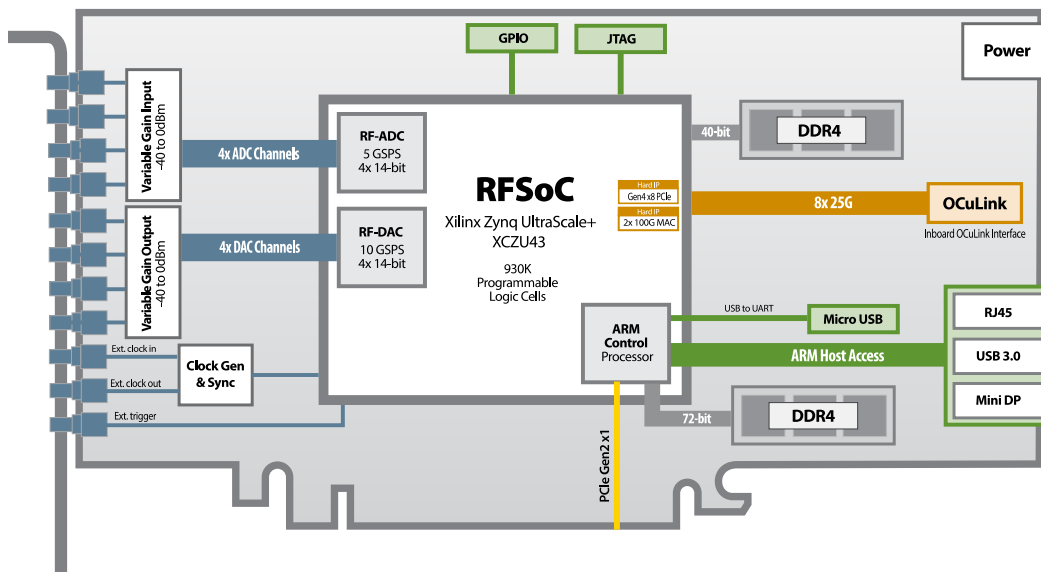


key features

Third Generation
Xilinx Zynq® Ultra-
Scale+™ RFSoc

Variable gain-
controlled RF
inputs & outputs

Support for
MathWorks®
tools



OCuLink Expansion Port

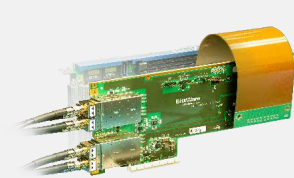
Get high-speed digital data on and off the RFX-8440 with support for:

- PCIe Gen4 x8 for NVMe or host attachment
- Dual 100GbE
- Custom lightweight protocols to connect to an FPGA processing board

Inquire about customized Molex connectors/cables as required for your application.

Additional Services

Take advantage of BittWare's range of design, integration, and support options



Customization

Additional specification options or accessory boards to meet your exact needs.



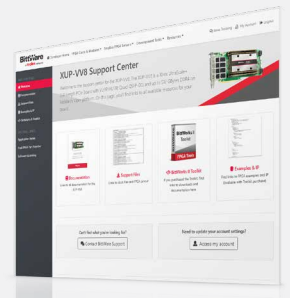
Server Integration

Available pre-integrated in our [TeraBox servers](#) in a range of configurations.



Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

FPGA	- Zynq UltraScale+ RFSoc - XCZU43 in an E1156 package - Core speed grade -2 - Contact BittWare for other FPGA options
Analog	- Optimized for L Band: 1GHz - 2GHz - Other analog configurations available; contact BittWare 4 x 5 GSPS 14-bit ADCs -40 to 0 dBm (default) 4 x 10 GSPS 14-bit DACs -40 to 0 dBm (default) - Programmable clocks - External reference and triggers - SSMC style connectors
On-board flash	- Flash memory for booting FPGA - Flash memory for ARM bootloader and OS image
External memory	16GB DDR4 processing system (ARM) memory with ECC 8GB DDR4 programmable logic memory with ECC
External digital interfaces	- Processing system - PCIe Gen2 x1 - RJ45 Ethernet - USB UART - USB 3.0 - Mini DisplayPort - Programmable logic - Up to 200 Gb/s via 8x 25G OCuLink - Hard IP support for dual 100GbE and PCIe Gen4

Cooling	- Standard: double-width passive heatsink - Optional: double-width active heatsink (with fan) - Optional: single-width passive heatsink
Electrical	- On-board power derived from 6-pin AUX connector or optionally from 12V PCIe slot connection - Power dissipation is application dependent - Typical max power consumption 50W
Environmental	Operating temperature: 5°C to 35°C
Quality	- Manufactured to ISO9001:2015 IPC-A-610-Class III - RoHS compliant - CE, FCC & ICES approvals
Form factor	¾-length, standard-height PCIe dual-slot card (x16 mechanical) - Supports standalone operation - RFX-8440 can be ordered as a TeraBox™ integrated server platform

Development Tools

FPGA development	BittWare provides a basic data capture and replay example utilizing the major interfaces of the product. Xilinx Vivado development tools are fully supported for development of custom designs.
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Deliverables

- RFX-8440 Analog Data Acquisition Card
- Data capture and relay example - Full source code
- 1-year hardware warranty
- Cable pack (optional)

To learn more, visit www.BittWare.com

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